

Global Standards for the Microelectronics Industry

DDR Compliance Testing Its time has come!

Barbara P. Aichinger FuturePlus Systems Corporation

Server Forum 2014

Copyright © 2014 FuturePlus Systems

DDR Compliance Testing

- If not then why now?
 - Continued growth and reliance on DDR memory
 - Critical applications increasing
 - Errors don't scale well
 - Large Data Centers replacing DIMMs every hour



Several Publications point to error rate much larger than **EXPECTED** DRAM Errors in the Wild: A Large-Scale Field Study Sigmetrics 2009

- ۲
- Cosmic Rays Don't Strike Twice: Understanding the Nature of DRAM • Errors and the Implications for System Design by Andy Hwang, Ioan Stefanovici and Bianca Schroeder)
- <u>A Field Study of DRAM Errors</u> 2012 by Sridharan, Liberty, RAS Architecture AMD
- Reliability, Serviceability and Availability: Intel XEON Processor E7 Family April 2014
- Characterizing Application Memory Error Vulnerability to Optimize • Datacenter Cost via Hetrogeneous-Reliability Memory June 2014 Microsoft
- <u>Avoiding server downtime from hardware errors in system memory</u> with HP Memory Quarantine HP Technology Brief January 2012
- Flipping bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors by Yoongu Ki, et al Carnegie Mellon University and Intel Labs July 2014



Open Compute Project

Ready Certification



- Compliant Certification
 - Will point at other standards...if they exist
- Certification labs
 - University of Texas San Antonio
 - ITRI (Taiwan)
- You can Join! www.OCP.com



National Institute of Standards and Technology

Information Technology Laboratories

 Cloud Computing Program

"...It is **considered critical** that government and industry begin adoption of this technology in response to difficult economic constraints.Cloud computing is currently being used; however, security, interoperability, and portability are cited as major barriers to broader adoption....The long term goal is to provide thought leadership and guidance around the cloud computing paradigm to catalyze its use within industry and government. NIST aims to **shorten the adoption cycle**.... NIST aims **to foster cloud computing systems and practices** that support **interoperability, portability, and security requirements** that are appropriate and achievable for important usage scenarios."



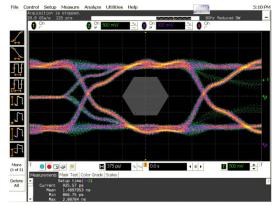
What would DDR4 Compliance Testing Look Like?

- DRAM specific
 - DIMM/SODIMM/LRDIMM
- Memory Controller specific
- The path between the two
- A Compliance Test Specification
 - T&M Vendors can produce MOI (Method of Implementation)
 - End users can then request this testing
 - Compliance Lab Testing



DDR4 Compliance Testing

- Memory Controller Specific
 - RX/TX eye specification
 - Bit Error Rate
 - Protocol Violations
 - Timing Violations



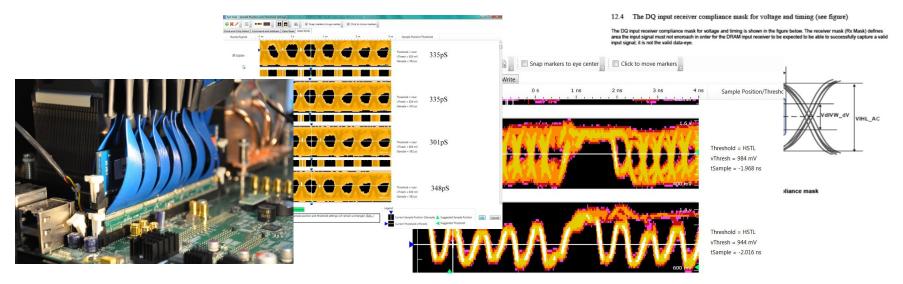
– Performance Specifications



Memory Controller RX/TX

Compliance Masks

- Measurement can be made with an interposer
 - Qualitative -> Quantitative



Memory Controller Protocol Violations

- The DDR4 JEDEC spec contains rules on event ordering
 - Examples
 - Do not ACTIVATE a bank that is already open
 - Do not PRECHARGE a bank that is already closed
 - Do not RD/WR a non open page



Memory Controller Timing Violations

- Clock edge boundary
- - Things can not be too close together or too far apart
 - Examples
 - tREFI Average refresh interval
 - tRC ACT ot ACT or REF
 - tMOD MRS to PDE
 - tCCD L RD to RD to Same Bank Group



65 violations identified with over 1000+ simultaneous checks

Select All	De-Select All	tCCD_L 5 nClks[2-15]
V1 - BD to BD to Same Bank Group	V31 - PRE or PREA to PDE	V4 - RD to RD Different Bank Group
✓ V2 - RD to WR to Same Bank Group	V32 - RD or RDA to PDE	tCCD_S 4 nClks[2-15]
✓ V3 - WR to WR Same Bank Group	✓ V33 - WR to PDE < tWRPDEN cc	
✓ V4 - RD to RD Different Bank Group	✓ V34 - WRA to PDE < tWRAPDEN cc	V5 - WR to WR Different Bank Group
✓ V5 - WR to WR Different Bank Group	✓ V35 - WR to PDE < tWRPBC4EN cc	tCCD_S 4 nClks[2-15]
✓ V6 - Min ACT to ACT Same Bank Group	✓ V36 - WR to PDE < tWRAPBC4EN_cc	
✓ V7 - Min ACT to ACT Different Bank Group	V37 - REF to PDE	V6 - Min ACT to ACT Same Bank Group
✓ V8 - 5 ACT < tFAWmin Same Rank	V38 - MRS to PDE	tRRD L 5 nClks[2-15]
✓ V9 - WR to RD Same Bank Group	✓ V39 - PRE, PREA to ACT, Other Commands	
✓ V10 - WR to RD Different Bank Group	V40 - ACT to PRE, PREA	V7 - Min ACT to ACT Different Bank Group
✓ V11 - RD to PRE or PREA Same Rank	✓ V41 - ACT to PRE or AutoPRE	tRRD_S 4 nClks[2-1023]
✓ V12 - WR to PRE(SB) or PREA (SR)	V42 - ACT to RD or WR	
✓ V13 - DLL Reset to any Command or CKE	✓ V43 - ACT to ACT or REF	
V13 ODT Enabled	✓ V44 - REF to non-DES	V8 - 5 ACT < tFAWmin Same Rank tFAW 20 nClks[2-63]
V14 - MRS to MRS	V45 - REF to REF Average Interval	tFAW 20 nClks[2-63]
V15 - MRS to Other Command or ODt High	V46 - REF to REF Maximum Interval	
V15 ODT Enabled	V47 - Read or Write to an Inactive Bank	V9 - WR to RD Same Bank Group
V16 - CA Bus and PAR_IN have odd # of 1's	V48 - Refresh to an Active Bank	tWTR_L 18 nClks[2-63]
V17 - 1st ZQCL after Reset Low to High	V49 - Activate to an Active Bank	
V17 ODT Enabled	V50 - MRS with an Active Bank	V10 - WR to RD Different Bank Group
✓ V18 - All but 1st ZQCL after Reset low to high	✓ V51 - Self Refresh Entry with an Active Bank	tWTR_S 15 nClks[2-63]
V18 ODT Enabled	✓ V52 - ZQCS or ZQCL with an Active Bank	
✓ V19 - Time from ZQCS to any Command	V53 - Read to Read (Different Rank)	V11 - RD to PRE or PREA Same Rank
V19 ODT Enabled	✓ V54 - Read to Read (Different DIMM)	tRTP 6 nClks[2-63]
V20 - Reset Low to High, then CKE Low to High	V55 - Read to Write (Different Rank)	
V20 ODT Enabled	✓ V56 - Read to Write (Different DIMM) V57 - Write to Read (Different Rank)	V12 - WR to PRE(SB) or PREA (SR)
✓ V21 - SRX to Command ✓ V22 - SRX to Non-Deselect	V57 - Write to Read (Different Rank)	tWR 25 nClks[2-127]
V22 - SRX to Non-Deselect	V59 - Write to Write (Different Rank)	
V24 - SRX to RD or CKE Low or ODT Hi	V60 - Write to Write (Different DIMM)	V13 - DLL Reset to any Command or CKE
V24 ODT Enabled	V61 - ODT high to Low Time < ODTH4_cc	tDLLK 597 nClks[2-1023]
V25 - SRE to SRX	✓ V62 - ODT high to Low Time < ODTH8_cc	
V26 - PDX to Non-Deselect	✓ V63 - PDE or SRE Followed by non-DES	
✓ V27 - CKE Minimum Pulse Width	✓ V64 - WRA, WRA to Command	V14 - MRS to MRS tMRD 8 pClks[2-15]
✓ V28 - PDE to PDX is less than tPDmin	✓ V65 - RDA to Command	tMRD 8 nClks[2-15]
✓ V29 - PDE to PDX is greater than tPDmax		
V30 - ACT to PDE		V15 - MRS to Other Command or ODT High tMOD 24 nClks[2-31]

Global Standards for the Microelectronics Industry

tZQinit 1024

nClks[2-2047]

.

Protocol and Timing Compliance 'in the wild'

ut - Configuration - Storage Qualification	Volations Courts Trigger Volations Setup WaveForm State Listing Storage Qualification Configuration							
- Trigger - Violations Setup tput - Run Log - Mode Register Set	Velation 1 R0 ■ RD to RD to Same Bank R1 ■ Group R2 ■ Total R3 ■	Violation 10 R0 WR to RD Different Bank R1 R2 Total 3556 Group R3 R	Violation 20 R0 R Reset Low to High, then R1 CKE Low to High R2 Total R3	Violation 29 R0 PDE to PDX is greater R1 than tPDmax R2 Total R3 R3 R3 R3 R3 R3 R3 R3	Violation 40 R0 ACT to PRE, PREA (Min) R1 R2 Total R3 R3			
- State Listing - WaveForm - Violations Counts - FPS Charts	Volation 2 R0 ■ RD to WR to Same Rank R1 ■ R2 ■ Total R3 ■	Violation 11 R0 R1 R2 R1 R1 R2 R1 R1 R3 R1 R1 R3	Violation 21 R0 = SRX to Command R1 = R2 = Total R3 =	Wolation 30 R0 ACT to PDE R1 R2 Total R3	Volation 41 R0 ACT to PRE or AutoPRE R1 Cotal R3			
	Violation 3 R0 WR to WR Same Bank Group R1 Total R2 Total R3	Violation 12 R0 WR to PRE(SB) or PREA R1 (SR) R2 Total R3	Violation 22 R0 = SRX to Non-Deselect R1 = R2 = Total R3 =	Volation 31 R0 PRE or PREAto PDE R1 R2 Total 3556 R3 R3	Volation 42 R0 ACT to RD or WR R1 R2 Total R3			
	Velation 4 R0 R1 RD to RD Different Bank R1 Total Group R2 Total R3	Violation 13 R0 DLL Reset to any Command R1 or CKE R3 R3	Violation 23 R0 SRX to ZQCL or ZQCS R1 R2 Total R3 •	Wolation 32 R0 RD or RDA to PDE R1 R2 Total R3	Volation 43 R0 ACT to ACT or REF R1 R2 Total R3			
	Violation 5 R0 ■ WR to WR Different Bank R1 ■ Group R2 ■ Total R3 ■	Violation 14 R0 MRS to MRS R1 R2 Total	Violation 24 R0 SRX to RD or CKE Low or R1 CODT H R2 Total R3	Violation 33 R0 WR to PDE <twrpden_cc< td=""> R1 R2 Total R3</twrpden_cc<>	Volation 44 R0 R REF to non-DES R1 R2 Total R3 R			
	Violation 6 R0 Min ACT to ACT Same Bank R1 Total Group R3 R	Violation 15 R0 MRS to Other Command or R1 R2 Total R3 R3	Violation 25 R0 ■ SRE to SRX R1 ■ R2 ■ Total R3 ■	Wolation 34 R0 WRA to PDE <twrapden_o r1<="" td=""> R2 R2 Total R3</twrapden_o>	Violation 45 R0 REF to REF Average R1 S556 Interval R3 R3			
	Violation 7 R0 Min ACT to ACT Different R1 Total R2 Total R3 R	Violation 17 R0 I 1st ZQCL after Reset Low R1 I to High R3 I	Violation 26 R0 PDX to Non-Deselect R1 R2 Total R3 R	Violation 37 R0 ■ REF to PDE R1 ■ R2 ■ Total R3 ■	Violation 46 R0 R REF to REF Maximum R1 Total R2 R Interval R3 R			
	Volation 8 R0 5 ACT < IFAWmin Same Rank R1 R2 Total R3	Violation 18 R0 All but 1st ZQCL after R1 Reset Low to High R2 Total R3	Violation 27 R0 ■ CKE Minimum Pulse Width R1 ■ R2 ■ Total R3 ■	Volation 38 R0 ■ MRS to PDE R1 ■ R2 ■ R3 ■	Volation 47 R0 Read or Write to an R1 Total R3 Rain R3			
	Violation 9 R0 ■ WR to RD Same Bank Group R1 ■ R2 ■ Total 3556	Violation 19 R0 ■ Time from ZQCS to any R1 ■ Command R2 ■ Total ■	Violation 28 R0 ■ PDE to PDX is less than R1 ■ tPDmin R2 ■ Total	Volation 39 R0 PRE, PREA to ACT, Other R1 Commands R2 Total	Volation 48 R0 ■ Refresh to an Active R1 ■ Bank R2 ■ Total			

JEDEC Specification Violation

Form Violation	s Setup Trigger	State Listing	Storage Qualification	Violations Counts Cor	figuration				
ic Notes								· · · ·	
	Gap of 4.67	′5 nS							
	1 nS								
Time	666932E	∑ 666933D	666933E	<u> </u>	X6669345	√666934 D	₹6669354	6669355	
Command	WR-R0	WR-R0	PRE-R1	PDE-CKE1	WR-RU	WR-R0	WR-R0	PRE-R0	
TRIGGER									
RA_VALID									
Bank Group	(1		2			1	×1	2	
Bank Address		Λ	2		1		Λ	2	
Address	(10158	10190	8190		X100E8	¥10130	¥10168	¥ 8168	
RAddr	(30A7	X30A7	χ5		X30AB	State # Time -12 66.385 ns -11 59.84 ns	Bank Group Row Address(RA) 1 30A7 1 30A3	Bank Address Addr Command 0 10028 WR-R0 3 10148 WR-R0	Violation(PV) Violat 0 0
CAddr	(158	×190			×	-10 52.36 ns -9 49.555 ns -8 44.88 ns	2 30AF 3 30AB 1 30A7	2 10078 WR-R0 1 30AB ACT-R0 0 100D0 WR-R0	0 0
PV							1 3047 1 5 1 30A7	0 80D0 RE-R1 0 10049 WR-R0	0
ViolationID				31		-5 30.855 ns -4 23.375 ns	3 30AB 1 30A7 1 30A7	2 1000 WR-R0 0 100E8 WR-R0 0 10158 WR-R0	0
			ACTIVE			-3 15.895 ns -2 1.87 ns -1 0.935 ns	1 30A7 0 30A7 2 5	0 10158 WR-R0 0 10190 WR-R0 2 8190 PRE-R1	0
R0 RPS						0 0 ns 1 5.61 ns	2 5 3 30AB	2 8190 PDE-CKE1 1 100E8 WR-R0	1 3
R1 RPS		X	ACTIVE		X	2 13.09 ns 3 19.635 ns 4 20.57 ns	1 30A7 1 30A7 2 D	0 10130 WR-R0 0 10168 WR-R0 2 8109 PRE-R0	0
R2 RPS	(X	λ		(5 27.115 ns 6 34.595 ns	0 30A3 1 30A7	3 10188 WR-R0 0 10150 WR-R0	0 0
R3 RPS	(χ	λ		6	7 42.075 ns 8 48.62 ns	1 30A7 0 30A7	0 10178 WR-R0 0 10100 WR-R0 0 10198 WR-R0	0
4099 ≑			Begin to End = 4	4,647 states [41.7	4495 µS] Begin	9 56.1 ns 10 71.06 ns	0 30A7 1 30A7	0 10160 WR-R0	0
						11 77.605 ns	0 30A7	0 10168 WR-R0	0

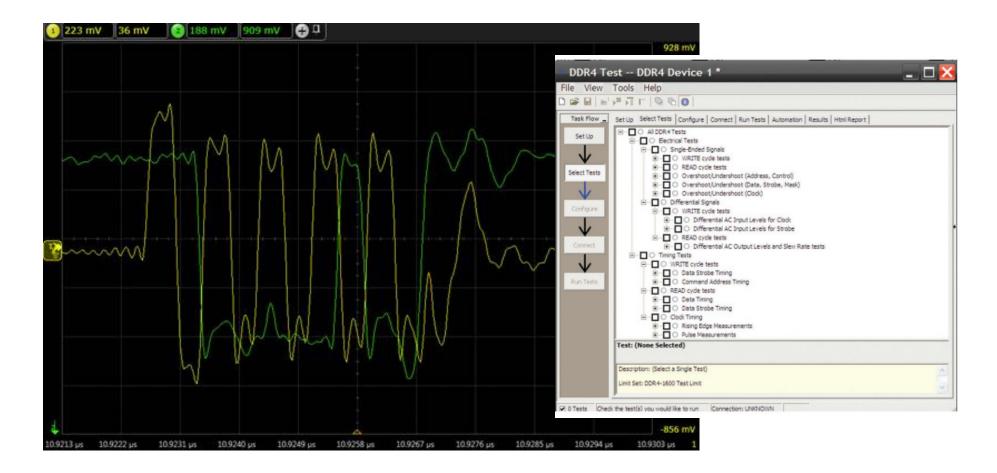
JEDEC

Memory Controller *Timing Violations*

- Timing that occurs between clock edges
 - Setup/Hold
 - Eye Mask
 - Jitter



Several Scope Vendors have DDR4 Compliance Products



JEDEC

Performance Metrics

BER testing at particular transfer rates

– 1E-16

- Which power management features are implemented
 - Is the clock stopped in Self Refresh?
 - Is Max Power Down implemented?

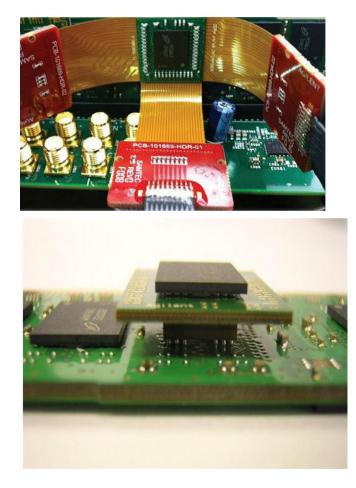


DDR4 Compliance Testing

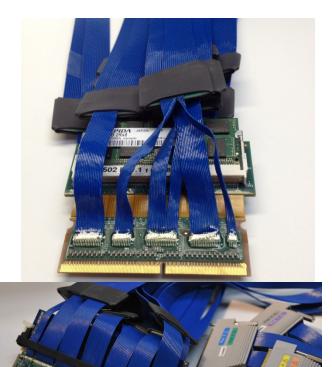
- DRAM Specific
 - DIMM/SODIMM/LRDIMM
 - RX/TX eye specification
 - Bit Error Rate
 - Data Integrity
 - Row Hammer (Excessive Activates)
 - Functional/Timing Verification
 - Performance Verification



Making the Measurement



Photos Courtesy of Keysight Technologies



Photos Courtesy of FuturePlus Systems

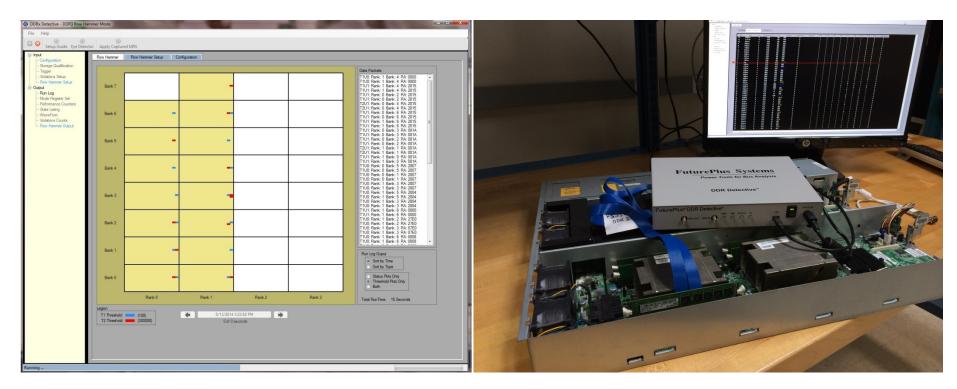


Row Hammer: Excessive Activates

- Yes its real.....easy to reproduce with software memory tests
- CMU study is the most recent technical paper on the topic
- Tools now look for it
- Data Centers are seeing it



Row Hammer Detection



Row Hammer detection feature of the DDR Detective® lists the row address when the number of ACT commands exceeds a threshold within 64ms. Two programmable thresholds are available

Testing a Server for Row Hammer using the DDR Detective® with software from ThirdIO

The electrical path between the DRAM and the Memory Controller

- End to End Measurements to verify channel integrity
- Require Slot/Channel loading configurations based on speed/eye size
- Memory channel layout/board files with simulation results?

Similar to what is done today with raw cards

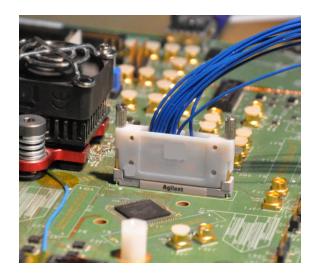


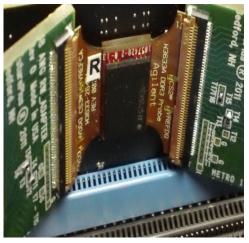
What about the LP DDR specifications?

- Many of the tests are applicable and can be reused
- Probing becomes more difficult but can be accomplished
- Measuring Power Management features becomes more critical



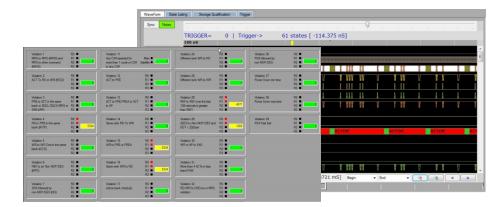
LPDDRx Compliance Test





JEDEC.





Advantages to having a Compliance Test Spec

- It is going to help our industry
 - End users are asking for this!
- Helps eliminate ambiguities in the specification
 - Ex: tREFI=Average Refresh time...over how many cycles?
- Makes high quality validation easier and less costly



My Contact Information

Barbara P Aichinger Vice President FuturePlus Systems Corporation Barb.Aichinger@FuturePlus.com Member JC42 and JC45

www.FuturePlus.com

