

W5643A DDR5 78-ball BGA Interposer

Overview

The W5643A DDR5 x4/x8 78-ball BGA interposer enables probing of embedded memory DRAM from the ball grid array with Keysight Technologies, Inc. U4164A logic analyzers. The Keysight W5643A DDR5 78-ball BGA interposers for logic analyzers enable viewing of traffic on industry standard DDR5 78-ball DRAMs with the Keysight U4164A logic analysis systems.

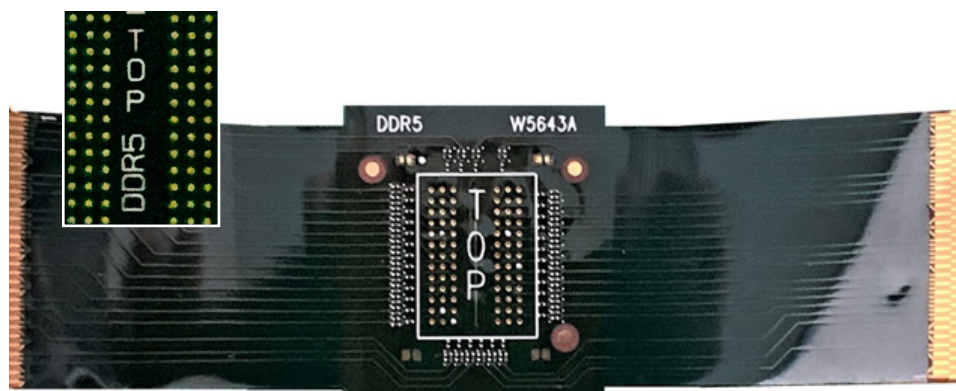
The W5643A DDR5 BGA interposers are designed to take full advantage of quad sample state mode on U4164A modules with Option 02G, requiring only a single probe point for up to four samples at two different thresholds. First in the industry, the W5643A DDR5 BGA interposers are thinner than any previous BGA interposers with a small KOV (keep out volume).

W5643A Series BGA interposers are designed to capture DDR5 protocol (CA/CS#/CK) for data rates up to 5Gb/s and capture DDR5 DQ at data rates up to 4Gb/s.¹



Key Benefits

- Probes a 78-ball DDR5 single channel x4 or x8 DRAM chip
- Access signals with one each U4208A and U4209A cables
- Measurement timing skews within +/- 25 psec
- Interposers are delivered with RC (resistor/capacitor) networks



¹ Maximum transfer rates are subject to variables in the signal integrity of the system under test and specifications of the U4164A logic analyzer module. U4164A specifications: minimum eye size of 100mV x 100ps at the RC network on the W5643A, maximum CK frequency of 2.5GHz, and maximum data rate of 4GT/s.

The DDR5 BGA Interposer Advantage

| Features | Benefits |
|--|--|
| Connects directly to the DDR5 BGA balls. | Eliminates reflections from mid-bus probing methods. Also eliminates design time, prototype builds, and trace routing required to design in alternative probing methods. |
| Supports/Enables: <ul style="list-style-type: none">• DDR5 78 ball single die, stacked, or quad x4, x8 DRAM at data rates up to 5Gb/s for protocol analysis and 4Gb/s DQ capture.• DDR eyescan display of DDR5 signals into logic analyzer module from BGA interposer• DDR5, decode, functional compliance and performance analysis using optional licensed software• Using APS (Advanced Probe Settings²) | Get complete signal access to the DDR5 signals critical to your debug. |
| Supports either leaded or lead-free solder. | Easily works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles. |
| Contract manufactures available for those without the in-house expertise or facilities for soldering BGAs. | Eliminates the need to develop BGA soldering expertise. |
| Flexible “wings” with ZIF connectors. | Ensures reliable connection to the ZIF probes. Enables placement of the probe cables around adjacent components. Minimizes the torque to the balls of the BGA. |

² To enable Advanced Probe Settings refer to **Technical Overview 5991-0799EN**.

Technical Characteristics

Keysight Technologies W5643A BGA Interposers enable probing of embedded DDR5 DRAM (x4 and x8) directly at the ball grid array using Keysight U4164A Logic Analyzers with option U4164A-02G.

Ball Count: 78

Package Size: maximum 11mm x 14mm³

Connectors: 2 Zero-Insertion Force (ZIF) Connectors

Key performance features:

- Probes a 78-ball DDR5 single channel x4 or x8 DRAM chip, JEDEC MO-207M footprint variation DT-z, with a maximum DRAM package size of 11mm x14mm
- Access signals with one each U4208A and U4209A cables with Zero-insertion force (ZIF) connectors. (sold separately).
- Measurement timing skews within +/- 25 psec achieved by matched trace lengths from DDR5 balls to test point
- Interposers are delivered with RC (resistor/capacitor) networks for logic analyzer probing installed on top of each DDR5 BGA interposer.
- W5643A ships with a riser to provide clearance for surrounding devices

W5643A includes:

- DDR5 x4/x8 78-ball BGA interposer
- DDR5 x4/x8 78-ball BGA riser

W5643A requires:

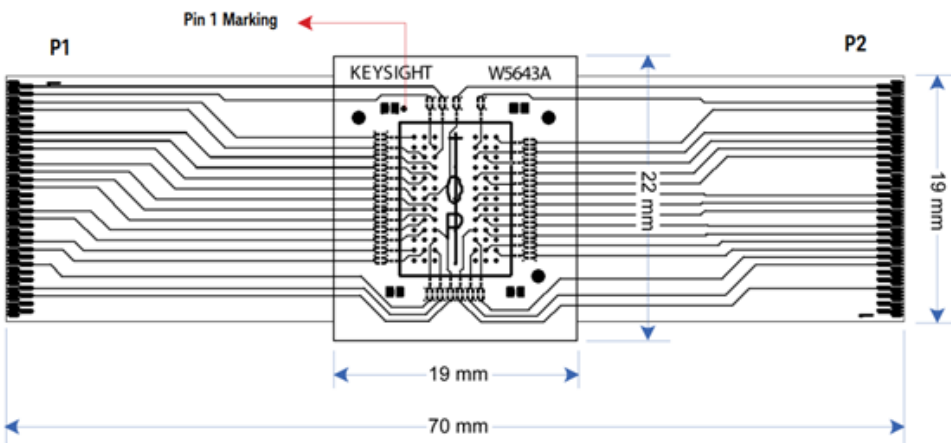
- Qty (1) U4208A Probe/cable, 61-pin ZIF, no RC, 160-pin direct connect to LA
- Qty (1) U4209A Probe/cable, 61-pin ZIF, no RC, 160-pin direct connect to LA
- Qty (1) U4164A logic analyzer module with option -02G speed grade option, chassis and either an embedded controller or host PC
- Qty (1) B4661A memory Analysis SW, no additional charge for base SW with default configurations and State mode tuning assistance.

Recommended for use with W5643A:

- Qty (1) B4661A-5FP/-5TP/-5NP DDR5 Analysis and Compliance SW licensed option for rapid navigation, debug, and validation of DDR5 system protocol.

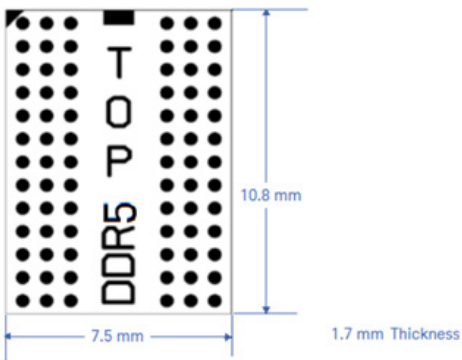
³ maximum of 11mm x 14mm DDR5 DRAM package can fit on top of DDR5 x4/x8 BGA interposer without an additional riser or socket (not provided) to provide clearance for the RC components.

Dimensional Drawings

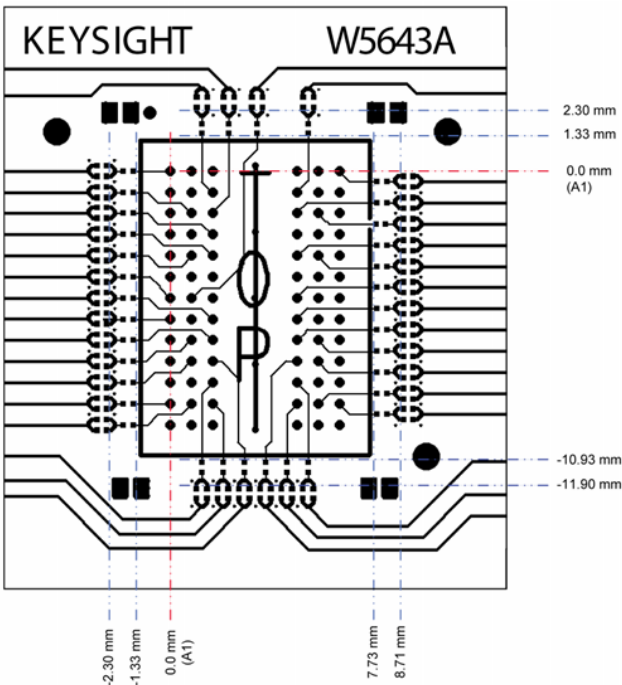


W5643A dimensions – Top view

0.5 mm thick in the BGA field, (not including BGA balls).



W5643A riser dimensions – Top view



- Pin A1 - Reference location at 0,0
- Edges of the pads for the tip R : ~0.1 mm height
- Edges of the pads for RC components : 0.2 mm height

Dimensions of 78-ball footprint on W5643A

Note: All measurements in millimeters

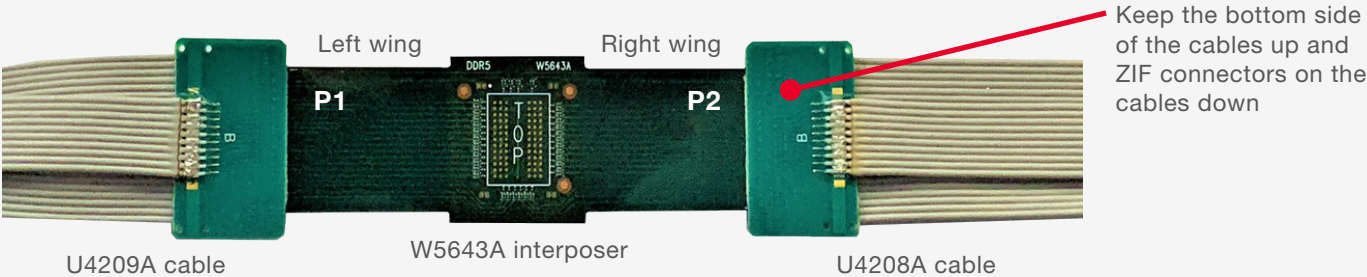
DDR5 78-ball Footprint Signal Mapping Into the W5643A

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---------|------|-------|---|---|---|--------|------|---------|---|
| A | LBDQ | GND | VPP | | | | ZQ | GND | LBDQS | A |
| B | VDD | VDDQ | DQ2 | | | | DQ3 | VDDQ | VDD | B |
| C | GND | DQ0 | DQS_t | | | | DM_n | DQ1 | GND | C |
| D | VDDQ | GND | DQS_c | | | | TDQS_c | GND | VDDQ | D |
| E | VDD | DQ4 | DQ6 | | | | DQ7 | DQ5 | VDD | E |
| F | GND | VDDQ | GND | | | | GND | VDDQ | GND | F |
| G | CA_ODT | MIR | VDD | | | | CK_t | VDDQ | TEN | G |
| H | ALERT_n | GND | CS_n | | | | CK_c | GND | VDD | H |
| J | VDDQ | CA4 | CA0 | | | | CA1 | CA5 | VDDQ | J |
| K | VDD | CA6 | CA2 | | | | CA3 | CA7 | VDD | K |
| L | VDDQ | GND | CA8 | | | | CA9 | GND | VDDQ | L |
| M | CAI | CA10 | CA12 | | | | CA13 | CA11 | RESET_n | M |
| N | VDD | GND | VDD | | | | VPP | GND | VDD | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |

| | |
|--|------------------------|
| | Quad-sampled Input |
| | Dual-sampled Input |
| | Clock/Qualifler Input |
| | Not connected in cable |

Connecting the W5643A to a U4164A logic analyzer with U4208A and U4209A probe/cables:

Attach the U4208A/9A cables inverted to the top side of the interposer



Top side view of the cable/interposer attachment



Bottom side view of the cable/interposer attachment

Signals and logic analyzer channel mapping to the W5643A

| Logic Analyzer Pod and its Channels | | Signals from U4208A Pod A |
|-------------------------------------|------|---------------------------|
| Pod 1 (Dual sampled) | 0 | |
| | 1 | |
| | 2 | |
| | 3 | CA3 |
| | 4 | CA13 |
| | 5 | CA9 |
| | 6 | RESET_n |
| | 7 | CA11 |
| | 8 | CA7 |
| | 9 | CA5 |
| | 10 | |
| | 11 | CA1 |
| | 12 | |
| | 13 | |
| | 14 | |
| | 15 | |
| | CLK | CK_c |
| | CLK# | CK_t |

| Logic Analyzer Pod and its Channels | | Signals from U4208A Pod A |
|-------------------------------------|------|---------------------------|
| Pod 3 (Dual sampled) | 0 | |
| | 1 | |
| | 2 | CA2 |
| | 3 | CA12 |
| | 4 | CA8 |
| | 5 | |
| | 6 | CA10 |
| | 7 | CAI |
| | 8 | |
| | 9 | |
| | 10 | CA6 |
| | 11 | CA4 |
| | 12 | CA0 |
| | 13 | ALERT_n |
| | 14 | CS_n |
| | 15 | CA_ODT |
| | CLK | |
| | CLK# | |

| Logic Analyzer Pod and its Channels | | Signals from U4208A Pod B |
|-------------------------------------|------|---------------------------|
| Pod 5 (Quad sampled) | 0 | |
| | 1 | |
| | 2 | DQ4 |
| | 3 | |
| | 4 | DQ6 |
| | 5 | |
| | 6 | DQS_c |
| | 7 | |
| | 8 | DQ0 |
| | 9 | |
| | 10 | LBDQ |
| | 11 | |
| | 12 | DQ2 |
| | 13 | |
| | 14 | DQS_t |
| | 15 | |
| | CLK | |
| | CLK# | |

| Logic Analyzer Pod and its Channels | | Signals from U4208A Pod B |
|-------------------------------------|------|---------------------------|
| Pod 7 (Quad sampled) | 0 | DQ5 |
| | 1 | |
| | 2 | DQ7 |
| | 3 | |
| | 4 | DQ1 |
| | 5 | |
| | 6 | DM_n |
| | 7 | |
| | 8 | LBDQS |
| | 9 | |
| | 10 | DQ3 |
| | 11 | |
| | 12 | |
| | 13 | |
| | 14 | MIR |
| | 15 | |
| | CLK | |
| | CLK# | |

W5643A is available in three different quantity options:

- W5643A-001 Qty (1), DDR5 BGA Interposer, 78-ball, 2-wing, connects to U4208A/U4209A
- W5643A-002 Qty (2), DDR5 BGA Interposer, 78-ball, 2-wing, connects to U4208A/U4209A
- W5643A-004 Qty (4), DDR5 BGA Interposer, 78-ball, 2-wing, connects to U4208A/U4209A

Typical configuration

Hardware:

- Qty (1) U4164A logic analyzer module (required)
 - Qty (1) U4164A-02G increase maximum speeds to 4GT/s (Required)
 - Qty (1) U4164A-008 increase maximum memory depth to 8Mb (Optional, user selects memory depth option)
- Qty (1) M9502A AXIe 2-slot chassis with ESM USB option (Can be substituted with M9505A 5-slot chassis)
- Qty (1) M9537A AXIe High Performance Embedded Controller, with keyboard, mouse and windows 10 options (Can substitute with Y1202A PCIe Cable, M9048A PCIe Desktop Adapter, and user supplied host Desktop.)

Software:

- Qty (1) B4661A Memory analysis SW (Required)
- Qty (1) licensed option: B4661A-5FP (Highly Recommended)

Probing Required:

- Qty (1) W4643A-001 quantity 1 DDR4 x4/x8 BGA interposer, 78-ball, 2-wing
- Qty (1) U4208A probe/cable, 61-pin ZIF, no RC, 160-pin direct connect to LA
- Qty (1) U4209A probe/cable, 61-pin ZIF, no RC, 160-pin direct connect to LA

Please refer to the Keysight W5643A DDR5 and W4640A/30A Series DDR4 BGA Interposers Installation Guide for details on installation.

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

